A Dataflow Architecture for Real-Time Full-Search Block Motion Estimation

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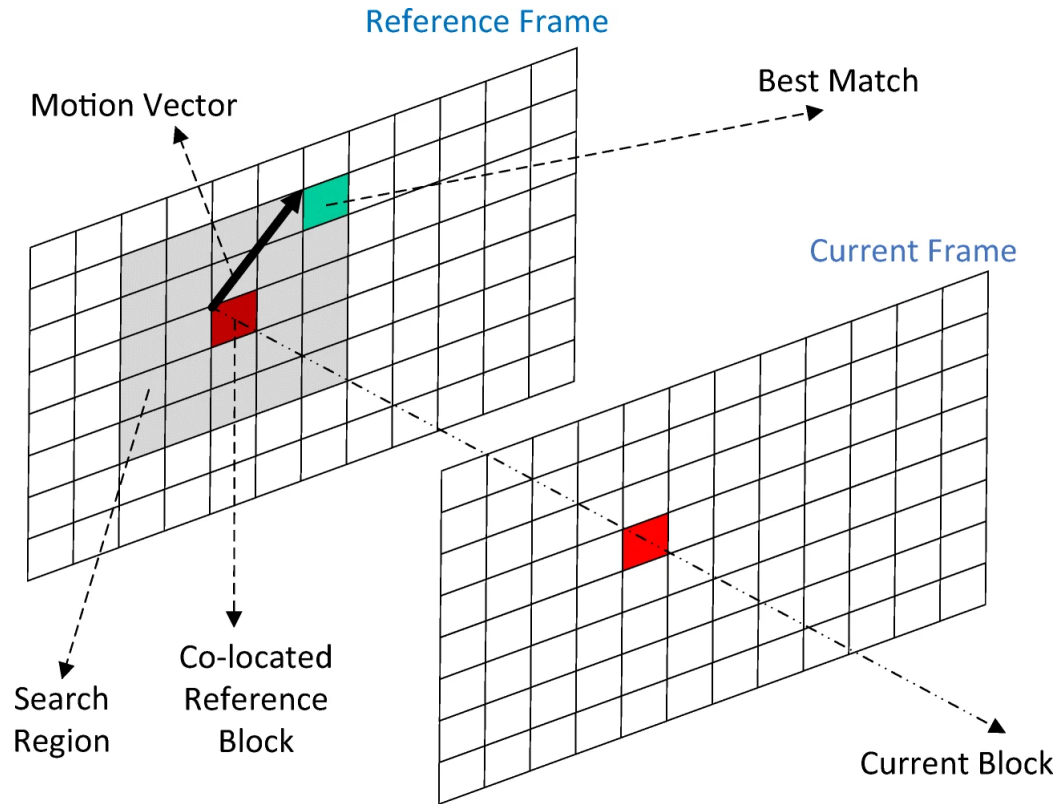
Motion estimation in video compression

- Exploits temporal redundancy in a video sequence
- The most computationally intensive and time-consuming operation
- Achieves high levels of compression
- Goal: to find similarities between blocks of pixels in different frames
- Different strategies to find the best match: trade-off between quality and speed



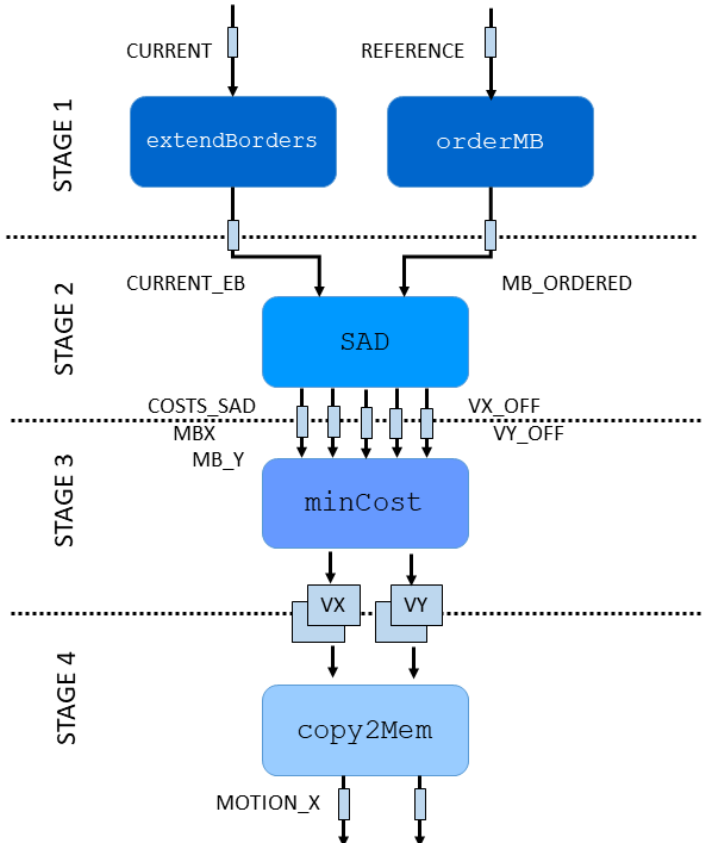
Source: Arnaudov, P., Ogunfunmi, T. Artificially Intelligent Adaptive Search Fast Motion Estimation Algorithm for HD Video. *J Sign Process Syst* **92,** 389–408 (2020).

Full-Search Block Matching Algorithm

- The most demanding algorithm for ME
- Nice testbed for FPGA technology
  - HLS design tools capabilities
  - Make the most of the available resources
- Goal: on-the fly ME computation in streams

	N=16, p=±16	N=16, p=±32
Integer operations per MB (SAD)	512	
#MBs comparisons	1.024	2.304
Integer operations per search window	524.288	≅1.180.000
Integer operations per frame (HD, 3600 MBs)	≅1.880M	≅4.247M
Integer oeprations per frame (FHD, 8100 MBs)	≅4.247M	≅9.555M

Overview of the accelerator



- Modeled using C++ subset for Vivado HLS
- Dataflow approach
- Minimize the use of BRAM memories
- Parameterized:
  - Search Area
  - Parallel MBs comparison

Results

Work	Platform	Clock (MHz)	MB size	Search Area	Resolution	FPS
[7]	Xilinx Spartan3	366.8	16x16	±16	HD	13.62
[5]	Altera Stratix	103.8	16x16	±16	HD	5.15
[9]	Xilinx XCV3200E	76.1	16x16	±16	HD	20.98
[12]	Altera Flex20KE	197	16x16	±16	HD	4.91
[3]	Xilinx Virtex 4	221.2	16x16	±16	HD	55.33
[6]	Xilinx Virtex 2	191	16x16	±16	HD	2.09
[2]	Xilinx Virtex 5 LX330T	125	8x8,16x6, 32x32,64x64	±64	FHD	26.9
	Virtex 6 LX240T					53.6
[1]	Xilinx Virtex 5	269.3	16x16	±32	FHD	31
						30
Ours	**Xilinx ZCU706 (Kintex-7)**	**115**	**16x16**	±16	**HD**	**247**
					FHD	**110**
				±32	**HD**	**124**
					FHD	**55**

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SEND QUESTIONS AND COMMENTS TO:

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